EEE6207-A1-ela16hcs

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EEE6207 - Dynamic Voltage Scaling

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Abstract

This report explains what dynamic voltage scaling (DVS) is and why it is a useful addition to a circuit. We also discuss how a DVS system can be constructed and how it works along with a case study example of a processor using DVS. Finally we discuss how and when these devices are feasible along with specific applications where DVS would be strongly considered.

1 Introduction

The majority of ICs (Integrated Circuits) and digital circuitry nowadays is constructed using CMOS technology. One appealing factor of CMOS logic is the low static power consumption due to the intrinsic insulated gate.[1] CMOS power dissipation can be split into 2 sections, static and dynamic power. Static power is from leakage currents through the device and dynamic power arises from device capacitors charging and discharging on clock cycles defined by $P_{Static} = I_{leak}V$ and $P_{dyn} = \alpha CV^2 f$ respectively. [2] As devices get faster the frequency increases dynamic power, as devices get smaller the leakage current gets larger increasing static power. [3]Reducing power consumption is a large modern concern and is one of the main features holding back technological advance. Reducing power is important as many devices depend on batteries for power. Smaller systems are strict with their battery sizes and must rely on other techniques to reduce power consumption. Device longevity is also affected by reducing power as a 15 degree rise in temperature doubles the chance of failure. [4]

And from the current as both pull-up/pull-down networks are momentarily on during a transition

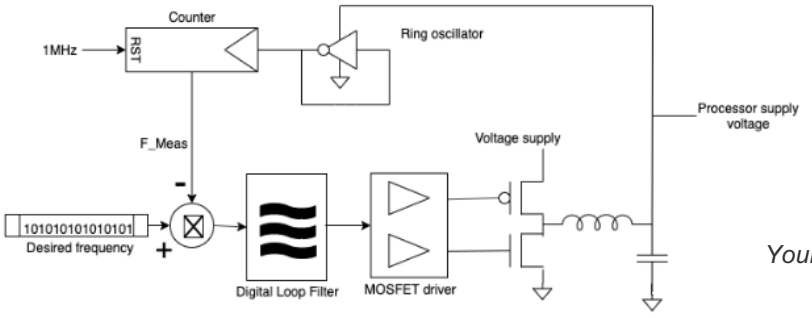
A DVS (Dynamic Voltage Scaling) system acts to vary the voltage supplied to the processor depending on load allowing for a system to work at the peak processing power whilst reducing power usage at non-peak usage. More advanced DVS systems also implement a variable frequency solution, for now this system is out of scope of a typical DVS.

good intro. Lots of useful information, relevant and well presented.

??? - surely the variable frequency goes hand-in-hand

2 Technical explanation

A common DVS architecture is shown in Figure: 1 [5]. It can be split into 6 distinct sections: A power supply, Ring oscillator, Counter, Binary comparison,



Your diagram?

Figure 1: Block diagram of a typical DVS system [5]

Digital Loop Filter and Mosfet driver. Each of these work in a digital and analog loop to generate the processor input voltage based on a value in memory (Desired frequency).

Starting with the power supply at the bottom right of Figure: 1, a buck converter is used to generate the output voltage given the input from a constant supply. If a linear system was used then all power would be dissipated that isn't used meaning no power is saved. A buck converter is used instead of a boost converter as we will always be stepping down the voltage from the supplied line. These inductor and capatictor components must be large enough to reduce ripple on the output as to not effect the processors operation. However the larger the capacitor the larger the transition time between a current voltage and a desired voltage and therefore the energy dissipated in this transition region as seen in Equation: 1 [5]. The larger this capacitance the slower the voltage can propagate from the device, we can work out a rough estimate for this time using $Q = CV$ and $I = \frac{Q}{T}$ giving $\tau = \frac{CV}{I}$ substituting in our circuit values we get Equation 2. The 2 in this equation comes from the triangular current operation of the buck convertor leading to an average current $I = 0.5 \cdot I_{max}$. For a $0.1V$ change using a capacitance of $1000\mu F$ and max current of $1A$ we get a response time of $200\mu S$ meaning no real time changes could be made. This means the best design would minimise capacitance whilst ensuring normal processor operation

OK. Whilst this is mechanism by which we can implement serving the frequency in a way which is mindful of the delays through logic as a function of Vdd, it is not telling me why.

$$E_{tran} = (1 - \eta) \cdot C \cdot |V_{Cur}^2 - V_{Des}^2| \tag{1}$$

$$\tau_{tran} = \frac{2 \cdot C}{.} I_max |V_{Cur} - V_{Des}| \tag{2}$$

This bucked voltage is fed into a ring oscillator as a power supply. The ring oscillator is simply a CMOS not gate fed into itself leading to the device oscillating as fast as possible defined by the time the CMOS gates charge and discharge. As the voltage supplied to the ring oscillator changes the CMOS capacitances charge and discharge faster leading to a higher frequency for a higher voltage and vice versa.

This variable frequency is then fed into a binary counter, this binary counter adds up each rising edge from the ring oscillator. With a 1MHz signal being fed into the reset pin the counter will add how many oscillations appear in $1\mu s$. This is therefore counting the ring oscillator frequency in MHz. The binary representation of this the then fed out as F_{Meas}.

A defined desired frequency is stored in a memory address available to the DVS system. This value is calculated, likely with a LUT, to generate the lowest possible frequency for the current system load. A logic block then calculates the difference between the desired frequency and F_{Meas} giving a frequency error.

This frequency error is fed into a digital loop filter. This filter is designed to be used in an closed loop feedback system constantly correcting the output generated based on error. This means the system is purely reactive to error present in the system. This loop filter generates a PWM signal output, from its current state modified by the error, to the MOSFET driver.

To close the analysis loop, the MOSTFET driver implements the required dead time and signal inversion required to drive the totem pole without shorting the supply. This totem pole is fed through an inductor and capacitor to create our entire buck converter system of charging and discharging LC circuit.

2.1 Case study

Advanced Micro Devices, Inc. (AMD) is a large chip manufacturing company, many of their products are used in portable and low energy devices such as laptops, in these devices low power consumption is one of the highest priorities. PowerNow! Is a DVFS system, meaning we can dynamically change the voltage and frequency of the processor[6]. PowerNow! Can modify the voltage between $0.925V$ and $2V$ and modify the frequency between $200MHz$ and $500MHz$ leading to an overall minimum power consumption of 8.56% of the maximum processor power. AMD's chipsets that use PowerNow! Are designed for use in laptops and systems with passive cooling needs. Whilst allowing for passive cooling when the chipsets are much more powerful, running a laptop on minimal processing needs such as low level programming or plain text editing the device could run for 10 times longer on the same battery whilst allowing for a more demanding application on the same processor. Realistically an AMD processor may only be used down to around $1.4V$ reducing power to 19.6% of its maximum.

The PowerNow! settings may be set using a 16 byte enhanced power management register (EPMR) model specific register (MSR). This data is set using drivers available for generic operating systems such as windows as well as real time operating systems (RTOS). PowerNow! Also allows for an automatic mode where the voltage and frequency are set dynamically without need for any verbose instruction from the drivers, this is calculated from how busy the processor currently is. The other two options allow for a high performance or power-saver mode depending on what the user would like.

Again, not actually telling me how/why

3 Feasibility study

In terms of DVS feasibility we have positives allowing for reduced power consumption in turn leading to increase battery life of portable devices. Whilst we are changing the processor power, we are doing so dynamically having little effect on maximum processing speeds. This does however have some disadvantages with it, although our DVS system allows for a dynamic range of processing ability, the processing ability is reduced in different ways, especially if a job switches between high and low load. A system using DVS also requires a processor with a programmable clock which in turn has its own disadvantages such as accuracy, space and required overheads to name a few. As DVS is another system required to be added into the circuit, the complexity and cost increases as such and as more processors are becoming multi-core and higher frequency the return is diminishing. A DVS system is also only useful if a system runs with different processing needs in its lifetime as if no switching of processor ability is needed for things such as dedicated multimedia or embedded systems the processor can be picked accordingly meaning DVS brings no advantage.

4 Conclusion

Overall a DVS system is very useful and should be a consideration for systems where power management if of a high priority such as portable technology. DVS systems should also be considered when a system has a largely varying load, some examples may be servers with time dependent loads to reduce cost of power given the large possible unused compute. Other devices that require a small form factor or have limited access to cooling such as server rack devices or space systems that cannot dissipate heat would find DVS systems a large advantage. Certain systems such as full time multimedia devices or embedded systems with a constant load may not benefit as much from DVS power savings compared to a good choice of processor.

References

[1] Kahng Dawon. Electric field controlled semiconductor device, August 27 1963. US Patent 3,102,230.

[2] Sparsh Mittal. A survey of techniques for improving energy efficiency in embedded computing systems. *arXiv preprint arXiv:1401.0765*, 2014.

[3] Wolfgang M Arden. The international technology roadmap for semiconductors—perspectives and challenges for the next 15 years. *Current Opinion in Solid State and Materials Science*, 6(5):371–377, 2002.

[4] Dave Anderson, Jim Dykes, and Erik Riedel. More than an interface-scsi vs. ata. In *FAST*, volume 2, page 3, 2003.

[5] Thomas D Burd and Robert W Brodersen. Design issues for dynamic voltage scaling. In *Proceedings of the 2000 international symposium on Low power electronics and design*, pages 9–14. ACM, 2000.

[6] Amd powernow! technology white paper, 2000.

I saw this talk - great conference - on the Cinqueterre!

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GRADEMARK REPORT

FINAL GRADE

72/100

GENERAL COMMENTS

Instructor

The problem with this report is that there is a lot of low level detail but the essential raison d'être is missing. If we monitor a processor's idle time at a particular clock frequency then we could, feasibly, reduce the clock frequency to a point where the active processes just fill the time available (i.e. idle time approaches 0). This does not save much. However, if we accompany the reduction in clock frequency with a reduction in Vdd (which will increase the critical delays) then we will get a significant reduction in energy expended. Tracking active processes will allow us to expend as little energy as possible for a given workload. There are issues with rapid transitions between voltages/frequencies which I might have expected to see mentioned.

PAGE 1

Text Comment. And from the current as both pull-up/pull-down networks are momentarily on during a transition

Text Comment. good intro. Lots of useful information, relevant and well presented.

Text Comment. ??? - surely the variable frequency goes hand-in-hand

PAGE 2

Text Comment. Your diagram?

Text Comment. OK. Whilst this is mechanism by which we can implement serving the frequency in a way which is mindful of the delays through logic as a function of Vdd, it is not telling me why.

PAGE 3

Text Comment. Again, not actually telling me how/why

Text Comment. I saw this talk - great conference - on the Cinqueterre!

RUBRIC: TECHNICAL REPORT RUBRIC 3.60 / 5

TECHNICAL (40%) 3 / 5

Marks will be awarded for the technical content - how fully does the assessment piece address the technical issues

EXCELLENT (5)	all of the technical issues are considered
GOOD (4)	Most of the technical issues are considered
REASONABLE (3)	the important and most relevant technical issues are considered
ACCEPTABLE (2)	A few important technical issues are considered. There may be errors or omissions
POOR (1)	Too few technical issues are considered to address the subject of the assessment or done so trivially
NON-SUBMISSION (0)	Non-submission/attempt or no technical issues identified

EXPLANATION (20%) 4 / 5

Marks will be awarded for the way in which the technical issues are addressed. How well are things explained

EXCELLENT (5)	The explanations make it easy for the reader to understand in detail the intricacies of the technical issues. Complex points are made comprehensible
GOOD (4)	Good explanations are given in the main but the reader may be left confused in a few places or a few important points will not be made
REASONABLE (3)	Reasonable explanations are given. The author may be confused and either not understand fully or not be able to convey this understanding to the reader
ACCEPTABLE (2)	Explanations will be just capable of conveying ideas to the user. There will be omissions or errors and a the reader may well be required to look at other sources to comprehend what is written
POOR (1)	Ideas will be jumbled or incomplete. Explanations will be riddled with errors or non-existent
NON-SUBMISSION (0)	Non-submission/attempt or explanations too confused to follow

ARGUMENTS (10%) 4 / 5

Marks will be awarded for the interpretation of the technical information when deciding the merits of technical aspects

EXCELLENT	Technical aspect are compared very well to give the reader a very good understanding of

(5)	the relative merits of various ideas - evidence will fully support the views expressed by the author
GOOD (4)	Technical aspect are compared well to give the reader a good understanding of the relative merits of various ideas - evidence, will in part, support the views expressed by the author.
REASONABLE (3)	Technical aspect are compared reasonably to give the reader a reasonable understanding of the relative merits of various ideas - evidence may be provided support the views expressed by the author. There may be inconsistencies and omissions.
ACCEPTABLE (2)	A few technical aspect will be compared to give the reader a just-acceptable understanding of the relative merits of various ideas - little evidence will be be provided support the views expressed by the author. There will be inconsistencies and omissions.
POOR (1)	Very limited technical aspect will be compared and the reader will not really be able to assess the relative merits of various ideas - no evidence will be be provided support the views expressed by the author. There will be inconsistencies and omissions.
NON-SUBMISSION (0)	Non-submission/attempt or very confused arguments unsupported by evidence

CONCLUSION (10%) 4 / 5

Marks will be awarded for the concluding comments. How well are the arguments and technical issues drawn together

EXCELLENT (5)	A well-rounded precis of the report that draws out the important aspect and provides a succinct view of the subject of the assignment
GOOD (4)	A good precis that leaves the reader with a good understanding of the subject matter of the assignment
REASONABLE (3)	A reasonable attempt at drawing together the various strands in the report. The reader may be left with an incomplete view.
ACCEPTABLE (2)	There will be an attempt at a conclusion but it is unlikely to add too much to a reader's understanding
POOR (1)	An inadequate conclusion that fails to address most of the issues in the report or to provide much understanding to the reader
NON-SUBMISSION (0)	Non-submission/attempt or a very confusing or too brief conclusion

ORGANISATION (10%) 4 / 5

Marks will be awarded for the appearance, clarity, layout, figures, accuracy, etc.

EXCELLENT (5)	A well-organised, accurate, and readable piece of work. Figures will be accurate, text will be well written. The layout will aid readability
GOOD	A well organised piece of work. There will be a few errors or inconsistencies

(4)

REASONABLE (3)	A reasonably organised piece of work. There will be problems in layout or accuracy. The language may be ambiguous in places and there may be formatting issues
ACCEPTABLE (2)	A just-acceptable organised piece of work. There will be problems in layout and accuracy. The language will be ambiguous in places and there will be formatting issues
POOR (1)	A poorly-organised piece of work. There will be significant problems in layout or accuracy. The language will be ambiguous in a number of places and there will be significant formatting issues
NON-SUBMISSION (0)	Non-submission/attempt. The layout will be very poor (no headings, poor figures, badly written).

REFERENCES (10%) 4 / 5

Marks will be awarded for the range of references used and their applicability

EXCELLENT (5)	A wide range of relevant references
GOOD (4)	A good range of relevant references. There may be unneeded references
REASONABLE (3)	A reasonable range of relevant references. There may be unneeded references or references may be used inappropriately.
ACCEPTABLE (2)	At least 4 references. References will be poorly used.
POOR (1)	Between 1 and 3 references. Alternatively, references are unused or badly used.
NON-SUBMISSION (0)	No references